11-15-00 A

JC948 U.S. PTO 11/14/00

JC688 U.S. PTO 09/712360 11/14/00

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. **0100.0001590** Total Pages 22
First Inventor or Application Identifier Daniel Eiref
Title Method and Apparatus for Passing Clear DVD Data in a Computer
Express Mail Label No. EL5042844669US

APPLICATION ELEMENTS *See MPEP chapter 600 concerning utility patent application contents.*	*ADDRESS TO:* **Assistant Commissioner for Patents Box Patent Application Washington, DC 20231**

1. ☒ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)
2. ☒ Specification *Total Pages* 13
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. ☒ Drawings *(35 USC 113) Total Sheets* 2
4. Oath or Declaration *Total Pages* 2
a. ☒ Newly executed (original or copy)
b. ☐ Copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 17 completed)
[Note Box 5 below]
i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ☐ Microfiche Computer Program *(Appendix)*

6. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
a. ☐ Computer Readable Copy
b. ☐ Paper Copy (identical to computer copy)
c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. ☒ Assignment Papers (cover sheet & document(s))
8. ☒ 37 CFR 3.73(b) Statement (when there is an assignee) ☒ Power of Attorney
9. ☐ English Translation Document (if applicable)
10. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
11. ☐ Preliminary Amendment
12. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
13. ☐ Small Entity Statement(s) ☐ Statement filed in Prior Application, Status still proper and desired.
14. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
15. ☐ Other

16. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information:*
☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No:
Prior Application Information: Examiner *Group / Art Unit:*

17. CORRESPONDENCE ADDRESS

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Name (Print/Type)	**John R. Garrett**	REGISTRATION NUMBER	**27,888**
Signature	John R Garrett	Date 11/14/00	

FEE TRANSMITTAL

Note: Effective October 1, 1997.
Patent fees are subject to annual revision.
TOTAL AMOUNT OF PAYMENT ($) 918.00

Filing Date	**Nov. 14, 2000**
First Named Inventor	**Daniel Eiref**
Group Art Unit	
Examiner Name	
Attorney Docket Number	**0100.0001590**

Complete if Known

Application Number	

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to

Deposit Account Number	50-0441
Deposit Account Name	**ATI Technologies, Inc.**

☒ Charge Any Additional Fee Required Under 37 CFR 1 16 and 1 17

☒ Charge the Issue Fee Set in 37 CFR 1 18 at the mailing of the Notice of Allowance

2. ☐ Payment Enclosed:
☐ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	**710.00**
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 710.00

2. CLAIMS

Claims	Extra	Fee from below	Fee Paid
Total **25**	(20 =) **5**	18	**90.00**
Indep **4**	(· 3 =) **1**		**78.00**
Multiple Dep.			

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim
109	80	209	40	Reissue independent claims over original patent
110	18	210	9	Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 168.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	
117	890	217	445	Extension for reply within third month	
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	**40.00**
146	710	246	355	Filing a submission after final rejection (37 CFR 1 129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR 1.129(b))	
Other fee (specify)					
Other fee (specify)					

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 40.00

SUBMITTED BY: MARKISON & RECKAMP, P.C.				Complete (if applicable)	
Typed or Printed Name	John R. Garrett			Reg. Number	27,888
Signature	John R Garrett	Date	11/14/00	Deposit Account User ID	50-0441

PATENT APPLICATION
DOCKET NO. 0100.0001590

In the United States Patent and Trademark Office

FILING OF A UNITED STATES PATENT APPLICATION

Title:

METHOD AND APPARATUS FOR PASSING CLEAR DVD DATA IN A COMPUTER

Inventors:

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Express Mail Label No. EL 504284669US

Date of Deposit: Nov. 14, 2000

I hereby certify that this paper is being deposited with the U.S. Postal Service "Express Mail Post Office to Addresses" service under 37 C.F.R. Section 1.10 on the 'Date of Deposit', indicated above, and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Name of Depositor: Rosalie Swanson
(print or type)

Signature: Rosalie Swanson

PATENT APPLICATION

0100.0001590

METHOD AND APPARATUS FOR PASSING CLEAR DVD DATA IN A COMPUTER

Field Of The Invention

The invention relates generally to methods and devices for passing clear DVD data (such as, DVD program streams). The present invention encompasses, in the most general terms, methods and devices for passing any form of encrypted data from any source.

Background Of The Invention

DVD technology is well known in the prior art. The DVD specification allows for single or dual-layered DVDs, and single-sided or double-sided DVDs. A single sided, dual layer DVD holds almost 8.5 Gigabytes, or about 8 hours of quality video and multi-channel soundtrack.

DVDs compress video information using MPEG-2 (Motion Pictures Experts Group), to minimize the amount of data required for video. The specification allows for up to 480 horizontal lines of resolution. This results in picture quality virtually free of video noise with a high level of detail and color fidelity.

When a computer or set-top box is used to display movies from a DVD, the DVD data process over the PCI bus in the computer or set-top box. After the DVD data is read over the PCI bus from a DVD source, it is the decrypted by the CPU. The CPU then re-encrypts the data for transmission over the PCI bus to an MPEG-2 decoder.

Because of the large amount of data involved in DVD, it places great demands on the computer of set-top box in terms of processing time. Therefore, there is a need in the prior art for a more efficient method of processing DVD data that also reduces the number of required computations by the computer or set-top box.

Brief Description Of The Drawings

The features of the present invention which are believed to be novel are set forth with particularity in the appended claims. The invention, together with further objects and advantages, can best be understood by reference to the following description taken in conjunction with the accompanying drawings, in the several figures of which like reference numerals identify like elements.

FIG. 1 is a block diagram illustrating a computer embodiment of the present invention.

FIG. 2 is a flowchart of the method of the present invention.

Detailed Description Of a Preferred Embodiment of The Invention

In general terms the present invention is a system for passing clear DVD (digital video disk) program streams from a CPU (central processing unit) to an MPEG-2 decoder. In the system the CPU connected to a first bus interface. A system memory is connected to the first bus interface via a memory bus. A second bus interface is connected to the first bus interface via a PCI (peripheral component interconnect) bus and a DVD data source is connected to the second bus interface. A packet data decoder is connected to the memory bus via a buffer. The CPU reads DVD data from the DVD data source across the PCI bus, decrypts the DVD data and creates a packet data, and sends

the packet data to the buffer via the memory bus. The MPEG-2 decoder receives the packet data, via the transport bus from the buffer. In more general terms, the present invention is a novel way of connecting two existing busses in a computer of set-top box.

A typical computer or set-top box has a central processing unit connected to a memory bus and a PCI bus by a north bridge, otherwise referred to as the host/PCI bridge, which is quad-ported. The CPU can read and write main memory, permitting a graphics device driver executing on the processor to access and manipulate graphics information stored in main memory that will be used by a graphics adapter. The processor can read and write an AGP graphics adapter's local memory and register set. This permits the graphics device driver executing on the processor to access and manipulate graphics information stored in the graphics adapter's local memory, and to control the adapter via its register set. The graphics adapter can read and write main memory. The graphics adapter doesn't have to keep all of the graphics information in its local memory. Rather, on an as-needed basis, its device driver can request that the operating system allocate some main memory for its use. The graphics adapter can then use its dedicated AGP bus into its assigned area of main memory for the storage and manipulation of graphics information.

DVD source data is compressed as it moves from a storage device over the PCI bus to main memory, and the bandwidth requirements remain modest. This is necessary because the PCI bus is a busy place and failure to keep up with video streaming cannot be tolerated. Once the compressed data is in main memory, it can then be transferred to an MPEG-2 decoder and displayed.

The peripheral component interconnect (PCI) is a popular high-bandwidth, processor-independent bus that can function as a peripheral bus. Compared with other common bus specifications, PCI delivers better system performance for high-speed I/0 subsystems (e.g., graphic display adapters, network interface controllers, disk controllers, and so on). The current standard allows the use of up to 64 data lines at 66 MHz, for a raw transfer rate of 528 MByte/s, or 4.224 Gbps. But it is not just a high

speed that makes PCI attractive. PCI is specifically designed to meet economically the I/0 requirements of modem systems; it requires very few chips to implement and supports other buses attached to the PCI bus.

The present invention is depicted as a block diagram in FIG. 1 and as a flow chart in FIG. 2. The present invention has general applicability, but is most advantageously used in a computer or set-top box. Inventively, in the computer or set-top box the system memory bus is connected to the transport stream input of the MPEG-2 decoder. The CPU writes program streams directly from the memory bus to the MPEG-2 decoder, thus avoiding the PCI bus, and thus requiring less computations and greater efficiency. Generally, some type of buffering is required to de-couple the CPU from the MPEG-2 decoder. The buffering is preferably FIFO (First In, First Out) element located either externally to the MPEG-2 decoder, or located in the MPEG-2 decoder's frame buffer.

FIG. 1 is a block diagram of the relevant portions of a computer for illustrating the present invention. The present invention is a system for passing clear DVD program streams from a CPU 100 to a decoder 118. The CPU 100 is connected to a first bus interface 102, referred to in the art as the north bridge. The present invention further encompasses the CPU 100 and the first bus interface 102 being integrated into a single chip. The system memory 101 is connected to the first bus interface 102 via a memory bus 103. The system bus 101 is typically formed from a plurality of dynamic random access memories (DRAM) 104, 106, 108. A second bus interface 112 is connected to the first bus interface 102 via a PCI bus 105. The second bus interface is generally referred to as the south bridge. A DVD data source 114 is connected to the second bus interface 112. The CPU 100 and the second bus interface 112 can also be integrated into a single chip.

A packet data decoder 118 is connected to the memory bus 103 via a buffer 110, such as a FIFO element. The CPU 100 reads DVD data from the DVD data source 114 across the PCI bus 105 and the north and south bridges 102, 112. The CPU 100 then decrypts the DVD data and creates packet data. The packet data is the sent to the buffer

110 via the memory bus 103. The decoder 118 receives the packet data, via the transport bus 140, from the buffer 110. The transport bus 140 consists of at least data lines 130, valid signal line 132, and clock line 134.

In one embodiment of the present invention the buffer 110 is a FIFO (first in first out) element. The FIFO element 110 generates a refill request interrupt on line 122 when the FIFO element 110 reaches a predetermined "almost empty" state. The CPU 100 forwards further packet data to the FIFO element 110 when the CPU 100 detects the refill request interrupt. The CPU 100 also is connected to the FIFO element 110 by a write enable line, which controls the write operation of the FIFO element 110.

The system further includes a free running clock 116 connected to the buffer 110 and to the decoder 118 for clocking the packet data out of the buffer 110. In a preferred embodiment the packet data is clocked out of the buffer in a range of 10Mb/sec to 60Mb/sec.

The method of the present invention is depicted in FIG. 2. In a first step for passing clear DVD program streams from a CPU to an MPEG-2 decoder the CPU reads DVD data from a DVD drive or source across a PCI bus. The CPU decrypts the DVD data and creates packet data therefrom in step 202. The packet data is then sent to the FIFO element via the north bridge and the memory bus. The CPU write enables the FIFO and then sends the packet data. In step 203 it is determined if the FIFO element is ready to receive packet data. Packet data is sent until the FIFO element is full. When the FIFO element is "full", the CPU waits to send more packet data (step 205). When the FIFO element is "almost empty" (a predetermined empty level), a refill request interrupt or signal is sent to the CPU. Upon receiving the refill request, the CPU sends additional packet data (step 204). After all packet data has been sent and the FIFO element is empty, an empty signal is sent from the FIFO element to the MPEG-2 decoder. The packet data is sent from the FIFO element, via a transport bus, to the MPEG-2 decoder in step 206. The data is clocked out of the FIFO element with a free running clock in the range of 10Mb/sec to 60Mb/sec. Finally, in step 208 the packet data is decoded and the

MPEG-2 data stream is produced. The MPEG-2 data stream is then processed to display the video content as is known in the art.

Therefore, the present invention overcomes the drawbacks of the prior art for a more efficient method of processing DVD data that also reduces the number of required computations by the computer or set-top box. The present invention also provides an advantage over the prior art in that clear DVD, as well as, other previously encrypted transport or program streams are not sent across the PCI bus.

The present invention is not limited to the particular details of the apparatus and method depicted and other modifications and applications are contemplated. Certain other changes may be made in the above-described method and apparatus without departing from the true spirit and scope of the invention herein involved. For example, other types of decoders, other than MPEG, can be used with the present invention. Furthermore, future versions of MPEG decoders, other than MPEG-2 can be used with the present invention. It is intended, therefore, that the subject matter of the present invention shall be interpreted as illustrative and not in a limiting sense.

What is claimed is:

1. A method for passing clear DVD program streams from a CPU (central processing unit) to an MPEG-2 decoder, comprising the steps of:

reading, via a CPU, DVD data from a DVD drive across a PCI (peripheral component interconnect) bus;

decrypting the DVD data in the CPU and creating packet data;

sending the packet data to a FIFO (first in first out) element via a memory bus;

forwarding the packet data from the FIFO element, via a transport bus, to an MPEG-2 decoder.

2. The method according to claim 1, wherein the FIFO element generates a refill request interrupt when the FIFO element reaches a predetermined "almost empty" state.

3. The method according to claim 2, wherein CPU forwards further packet data to the FIFO element when the CPU detects the refill request interrupt.

4. The method according to claim 1, wherein the method further includes clocking the data out of the FIFO element with a free running clock.

5. The method according to claim 4, wherein the packet data is clocked out of the FIFO element in a range of 10Mb/sec to 60Mb/sec.

6. A method for passing clear DVD program streams from a CPU (central processing unit) to an MPEG type decoder, comprising the steps of:
decrypting the DVD data in the CPU and creating packet data;
sending the packet data to a buffer via a memory bus;
forwarding the packet data from the buffer, via a transport bus, to an MPEG type decoder.

7. The method according to claim 6, wherein the MPEG type decoder is an MPEG-2 decoder.

8. The method according to claim 6, wherein the buffer is a FIFO (first in first out) element.

9. The method according to claim 8, wherein the FIFO element generates a refill request interrupt when the FIFO element reaches a predetermined "almost empty" state.

10. The method according to claim 9, wherein CPU forwards further packet data to the FIFO element when the CPU detects the refill request interrupt.

11. The method according to claim 6, wherein the method further includes clocking the data out of the FIFO element with a free running clock.

12. The method according to claim 11, wherein the packet data is clocked out of the FIFO element in a range of 10Mb/sec to 60Mb/sec.

13. A system for passing clear DVD program streams from a CPU (central processing unit) to a decoder, comprising:

a CPU connected to a first bus interface;

system memory connected to the first bus interface via a memory bus;

a second bus interface connected to the first bus interface via a PCI (peripheral component interconnect) bus;

a DVD data source connected to the second bus interface; and

a packet data decoder connected to the memory bus via a buffer;

wherein the CPU reads DVD data from the DVD data source across the PCI bus, decrypts the DVD data and creating packet data, sends the packet data to the buffer via the memory bus, and wherein the decoder receives the packet data, via the transport bus, from the buffer.

14. The system according to claim 13, wherein the buffer is a FIFO (first in first out) element.

15. The system according to claim 14, wherein the FIFO element generates a refill request interrupt when the FIFO element reaches a predetermined "almost empty" state.

16. The system according to claim 15, wherein CPU forwards further packet data to the FIFO element when the CPU detects the refill request interrupt.

17. The system according to claim 13, wherein the system further includes a free running clock connected to the buffer for clocking the packet data out of the buffer.

18. The system according to claim 17, wherein the packet data is clocked out of the buffer in a range of 10Mb/sec to 60Mb/sec.

19. A set-top box that passes clear DVD program streams from a CPU (central processing unit) to an MPEG type decoder, comprising:

a CPU connected to a first bus interface;

system memory connected to the first bus interface via a memory bus;

a second bus interface connected to the first bus interface via a PCI (peripheral component interconnect) bus;

a DVD data source connected to the second bus interface; and

an MPEG type decoder connected to the memory bus via a buffer;

wherein the CPU reads DVD data from the DVD data source across the PCI bus, decrypts the DVD data and creats packet data, sends the packet data to the buffer via the memory bus, and wherein the MPEG type decoder receives the packet data, via the transport bus, from the buffer.

20. The set-top box according to claim 19, wherein the buffer is a FIFO (first in first out) element.

21. The set-top according to claim 20, wherein the FIFO element generates a refill request interrupt when the FIFO element reaches a predetermined "almost empty" state.

22. The set-top according to claim 21, wherein CPU forwards further packet data to the FIFO element when the CPU detects the refill request interrupt.

23. The set-top according to claim 19, wherein the system further includes a free running clock connected to the buffer for clocking the packet data out of the buffer.

24. The set-top according to claim 23, wherein the packet data is clocked out of the buffer in a range of 10Mb/sec to 60Mb/sec.

25. The set-top according to claim 19, wherein the MPEG type decoder is an MPEG-2 decoder.

METHOD AND APPARATUS FOR PASSING CLEAR DVD DATA IN A COMPUTER

Abstract Of The Disclosure

The system is for passing clear DVD program streams from a CPU (central processing unit) to an MPEG-2 decoder. In the system the CPU is connected to a first bus interface. A system memory is connected to the first bus interface via a memory bus. A second bus interface is connected to the first bus interface via a PCI (peripheral component interconnect) bus and a DVD data source is connected to the second bus interface. A packet data decoder is connected to the memory bus via a buffer. The CPU reads DVD data from the DVD data source across the PCI bus, decrypts the DVD data and creates a packet data, and sends the packet data to the buffer via the memory bus. The MPEG-2 decoder receives the packet data, via the transport bus, from the buffer. In more general terms, the system connects two existing busses in a computer of set-top box.

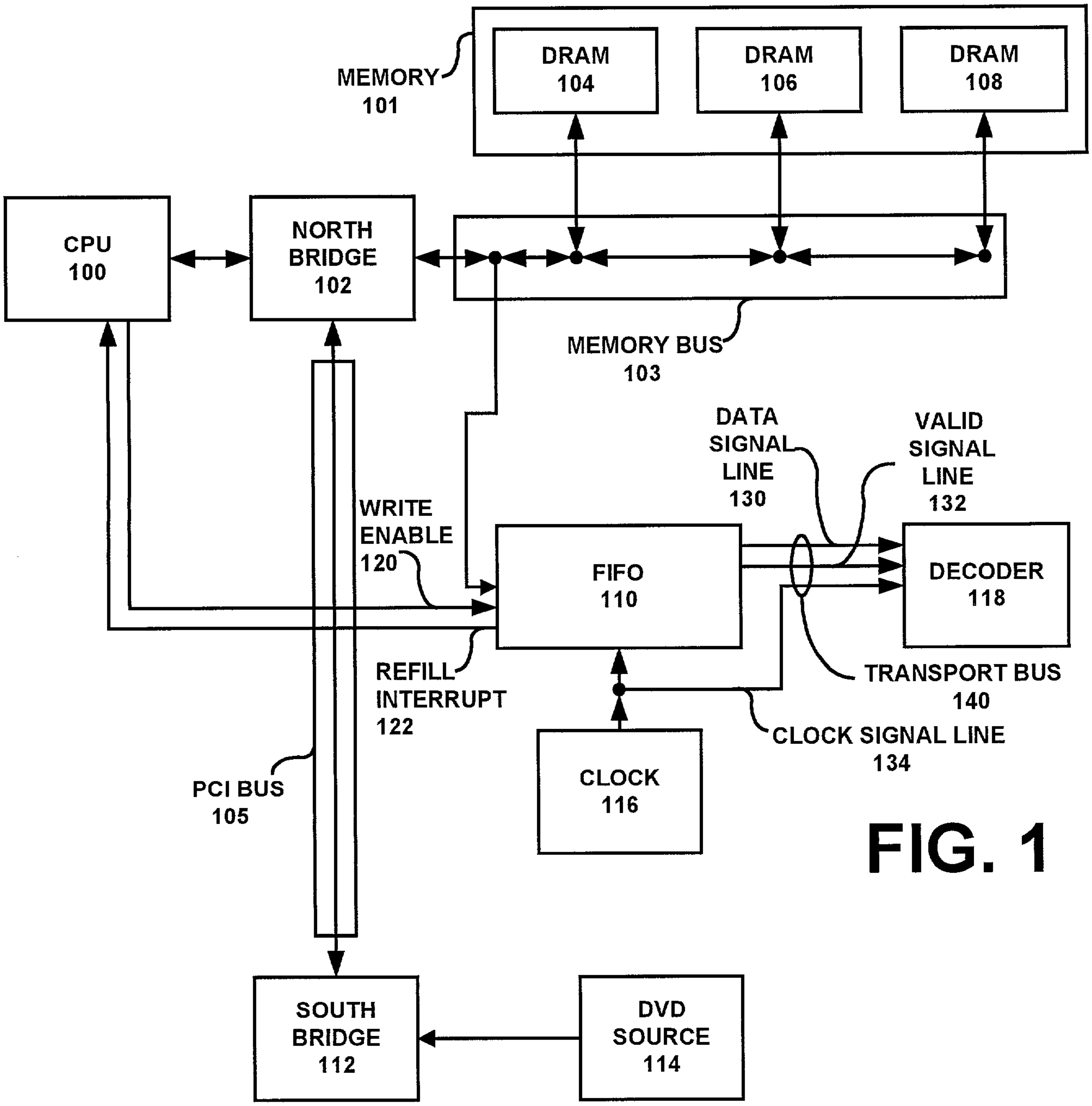
MEMORY
101
DRAM
104
DRAM
106
DRAM
108
CPU
100
NORTH
BRIDGE
102
MEMORY BUS
103
DATA
SIGNAL
LINE
130
VALID
SIGNAL
LINE
132
WRITE
ENABLE
120
FIFO
110
DECODER
118
REFILL
INTERRUPT
122
TRANSPORT BUS
140
CLOCK SIGNAL LINE
134
PCI BUS
105
CLOCK
116
SOUTH
BRIDGE
112
DVD
SOURCE
114

FIG. 1

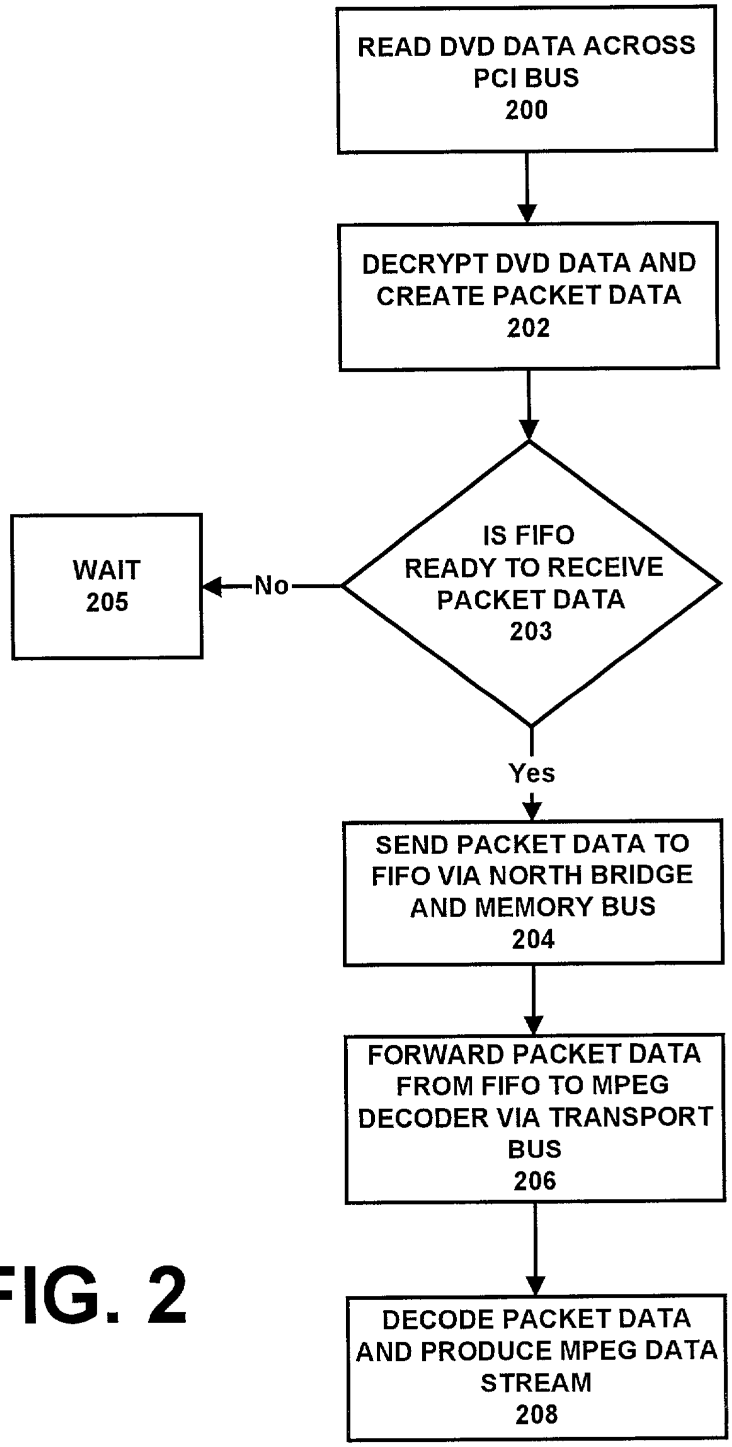
READ DVD DATA ACROSS PCI BUS
200
DECRYPT DVD DATA AND CREATE PACKET DATA
202
IS FIFO READY TO RECEIVE PACKET DATA
203
No
WAIT
205
Yes
SEND PACKET DATA TO FIFO VIA NORTH BRIDGE AND MEMORY BUS
204
FORWARD PACKET DATA FROM FIFO TO MPEG DECODER VIA TRANSPORT BUS
206
DECODE PACKET DATA AND PRODUCE MPEG DATA STREAM
208

FIG. 2

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION

(37 CFR 1.63)

☒ Declaration Submitted with Initial Filing, OR
☐ Declaration Submitted after Initial Filing
(surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number 0100.0001590
First Named Inventor Daniel Eiref
COMPLETE IF KNOWN
Application Number
Filing Date
Group Art Unit
Examiner Name

As a below named inventor, I hereby declare that:
My residence, post office address, and citizenship are as stated below next to my name.
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **Method and Apparatus for Passing Clear DVD Data in a Computer**
the specification of which:
☒ is attached hereto.
☐ was file on (MM/DD/YYYY) as United States Application Number or PCT International Application Number and was amended on (MM/DD/YYYY) (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.
I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Data (MM/DD/YYYY)

☐ Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)

☐ Additional U.S. or PCT international application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Name	Registration Number	Name	Registration Number
John R. Garrett	27,888	Christopher J. Reckamp	34,414
Daniel C. Crilly	38,417		
Sally Daub	41,478		

☐ Additional registered practitioner(s) named on supplemental Registered Practitioner Information sheet PTO/SB/02C attached hereto.

Direct all correspondence to:

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Chicago, Illinois 60606-0229
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Facsimile: 312-939-9828

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])		Family Name or Surname		
Daniel		**Eiref**		
Inventor's Signature	Daniel Eiref		**Date**	11/3/00
Residence	City: **Cambridge**	State: **MA**	Country: **USA**	Citizenship: **USA**
Post Office Address	**108 Lexington Avenue**			
City: Cambridge	State: **MA**	ZIP: **02138**	Country: **USA**	

Name of Additional Joint Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])		Family Name or Surname		
Leon		**Hesch**		
Inventor's Signature	Leon Hesch		**Date**	11/3/2000
Residence	City: **Littleton**	State: **MA**	Country: **USA**	Citizenship: **USA**
Post Office Address	**1 Kimball Street**			
City: Littleton	State: **MA**	ZIP: **01460**	Country: **USA**	

Name of Additional Joint Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])		Family Name or Surname		
Inventor's Signature			**Date**	
Residence	City:	State:	Country:	Citizenship:
Post Office Address				
City:	State:	ZIP:	Country:	

☐ Additional inventors are being named on the _____supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto.